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FIG. 1

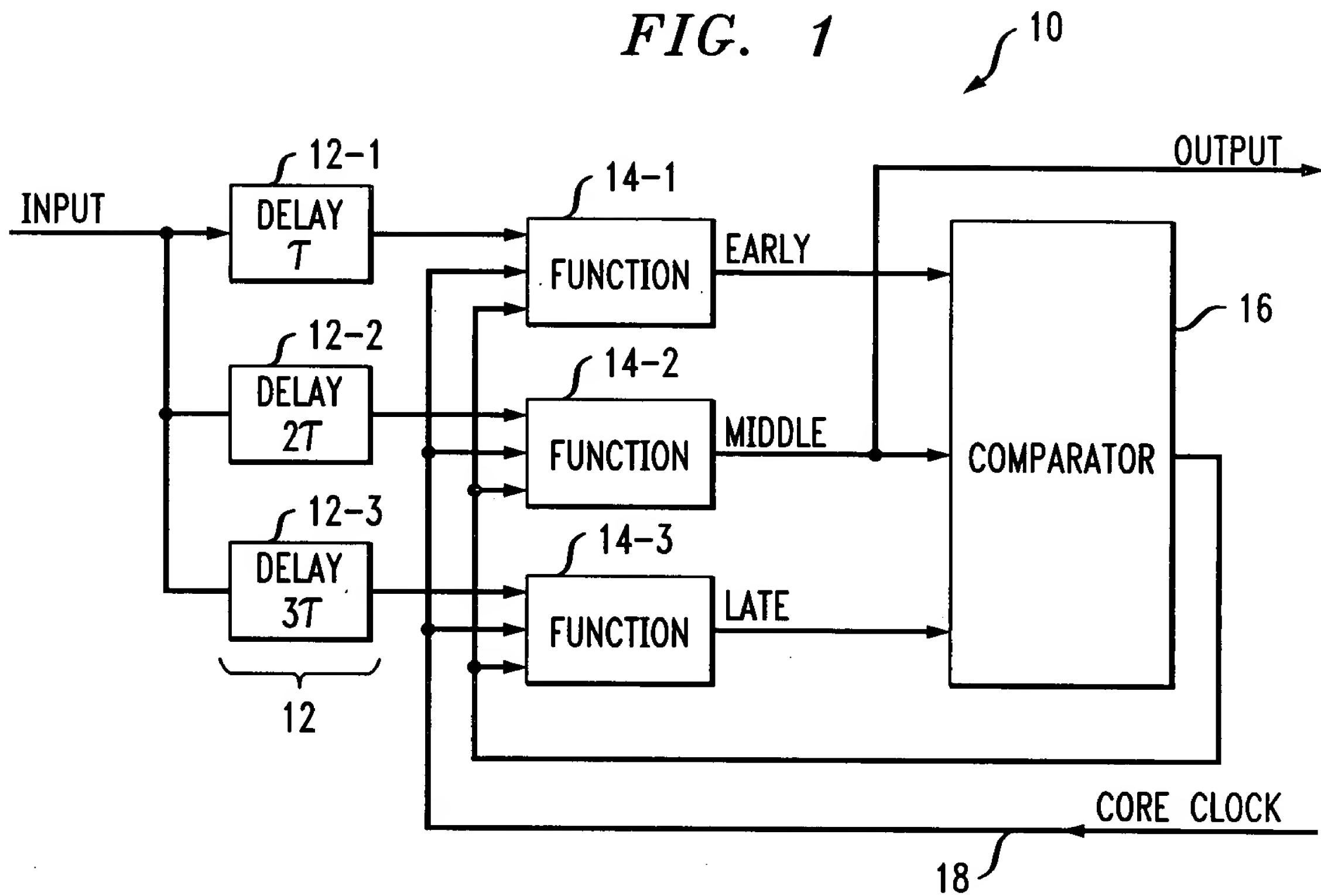
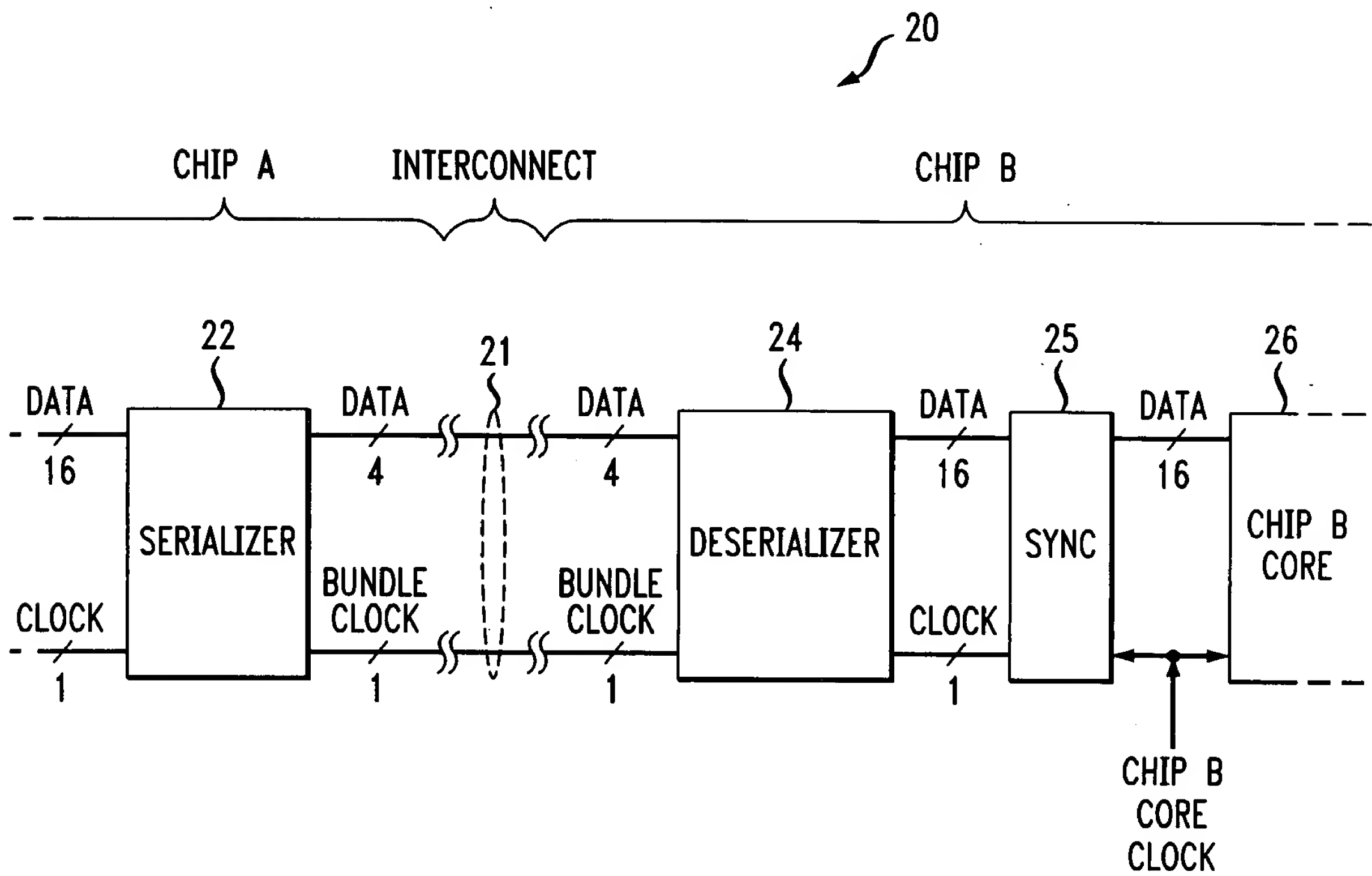
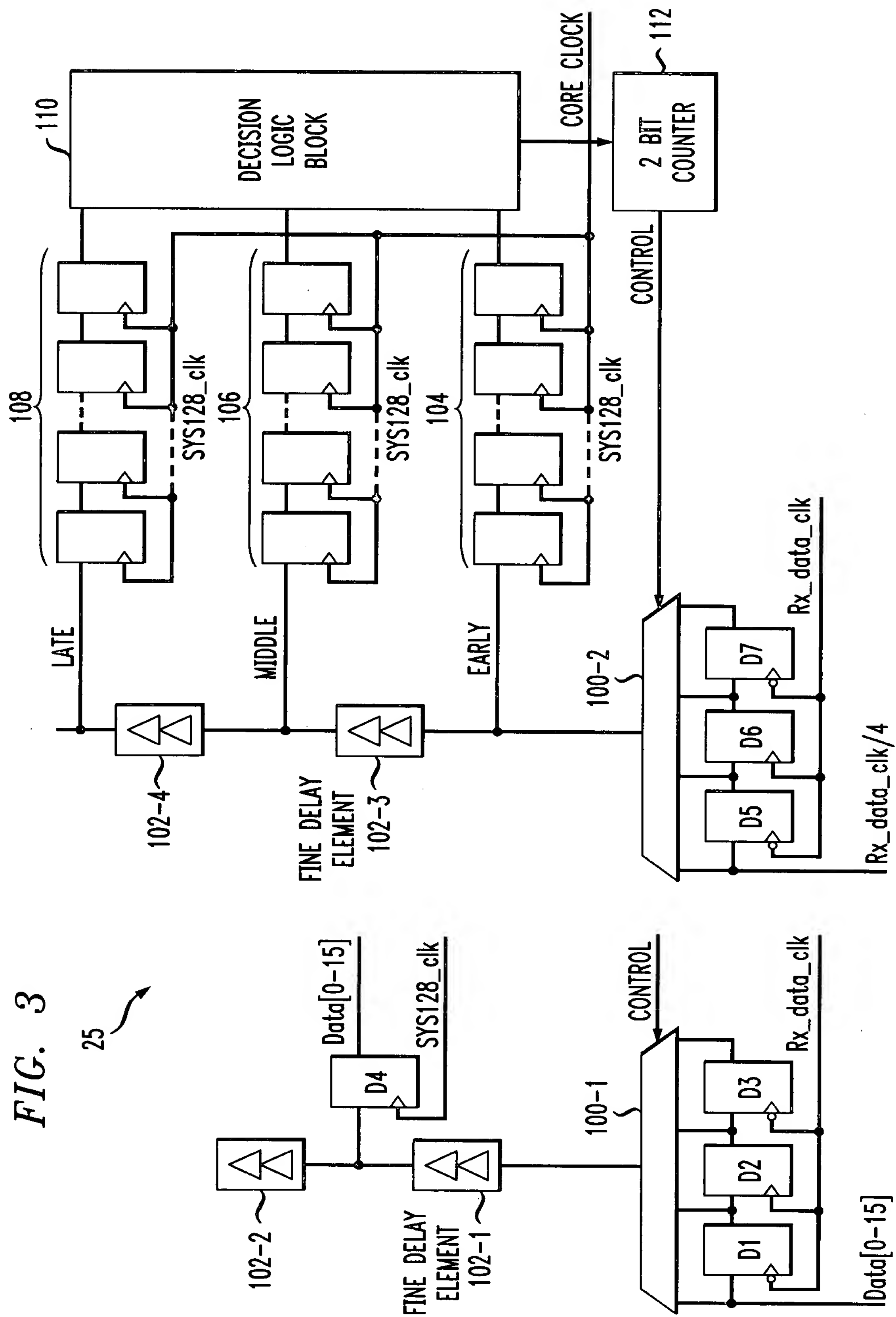


FIG. 2



**FIG. 3**

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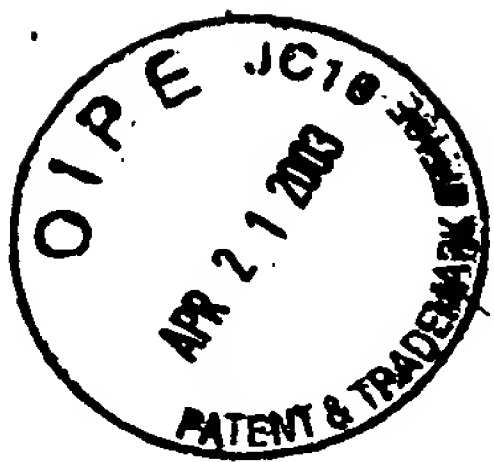
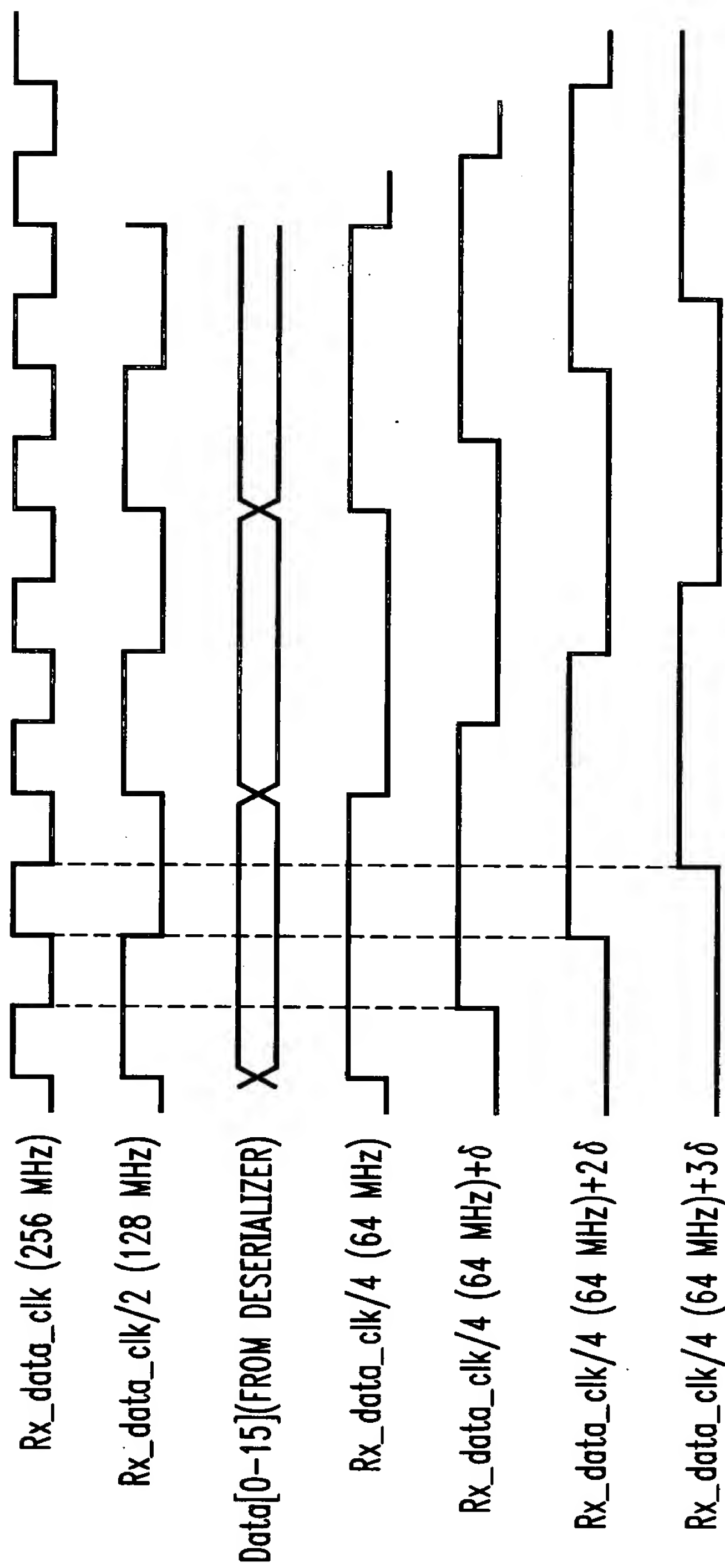


FIG. 4



$\delta$  = DELAY = 1/2 PERIOD OF Rx\_data\_clk

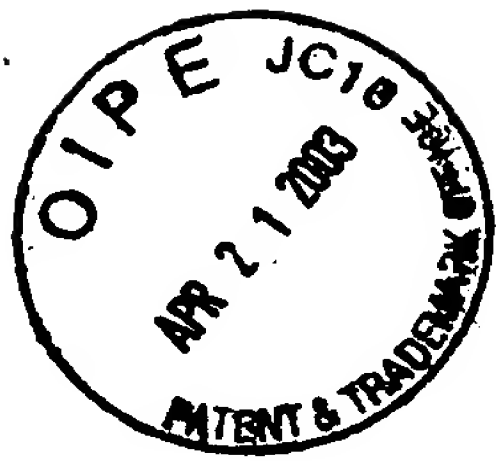


FIG. 5A

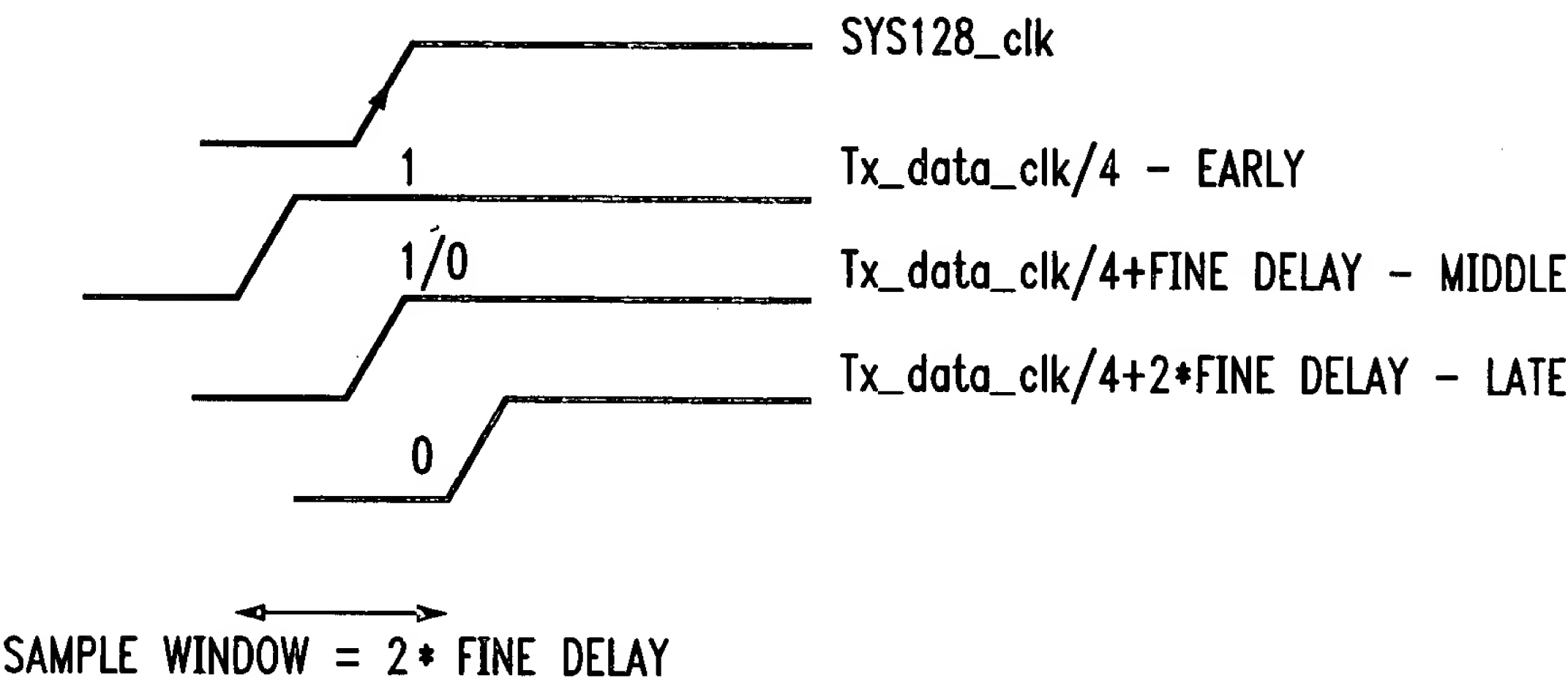


FIG. 5B

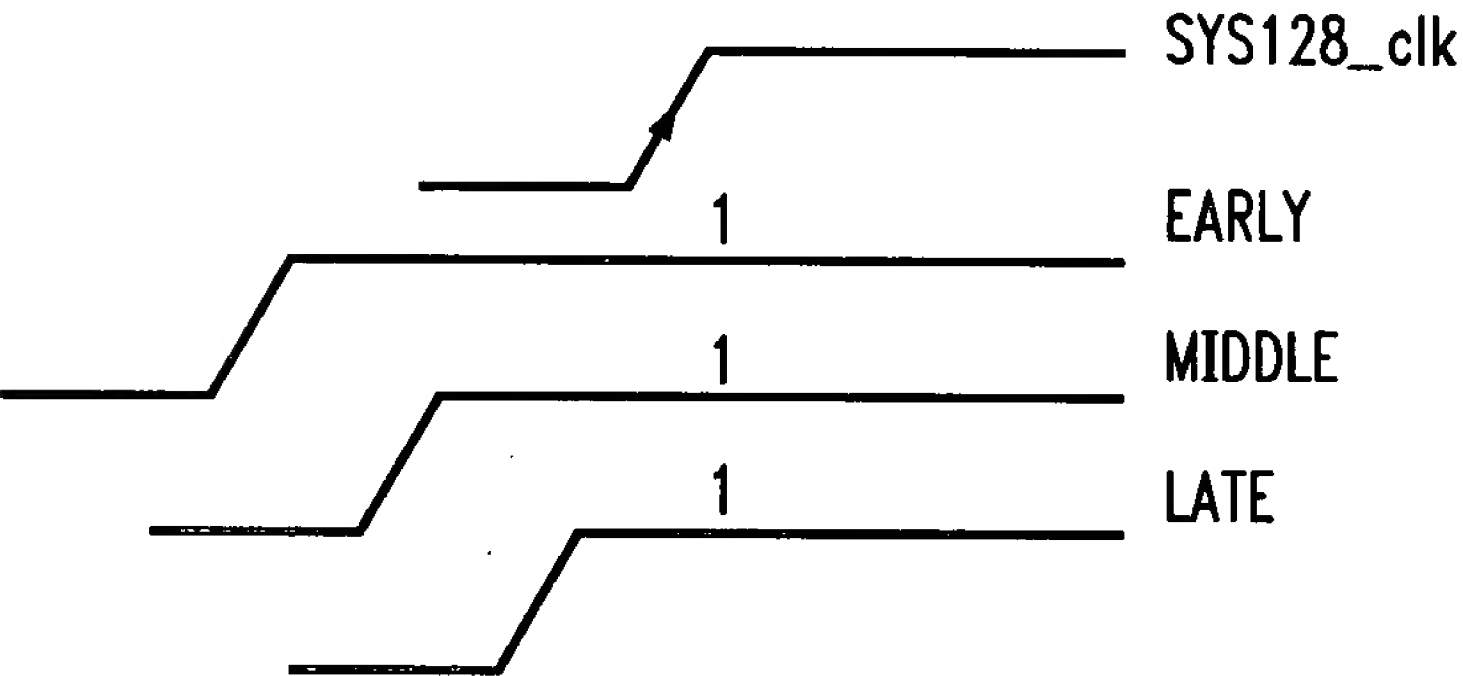
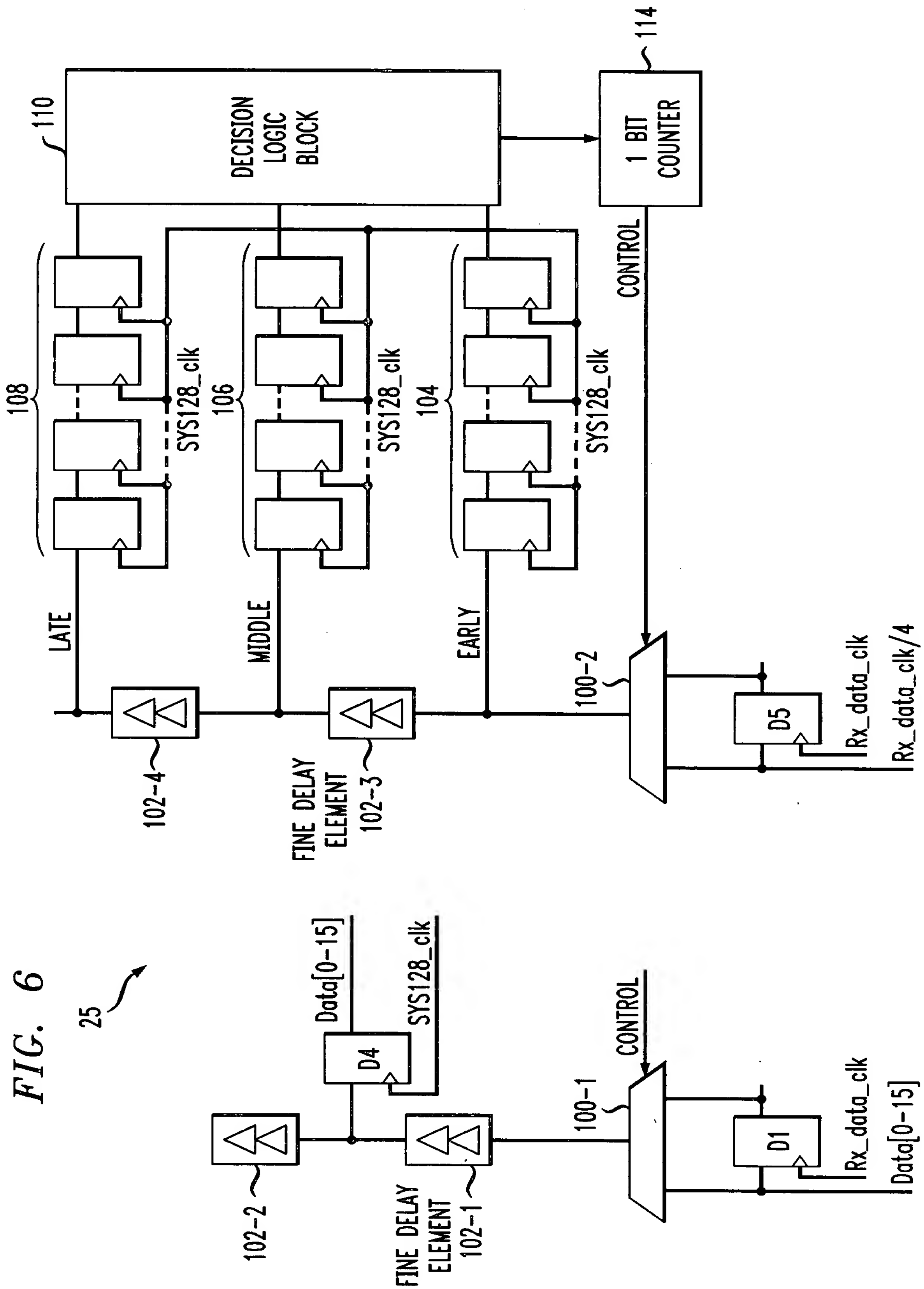
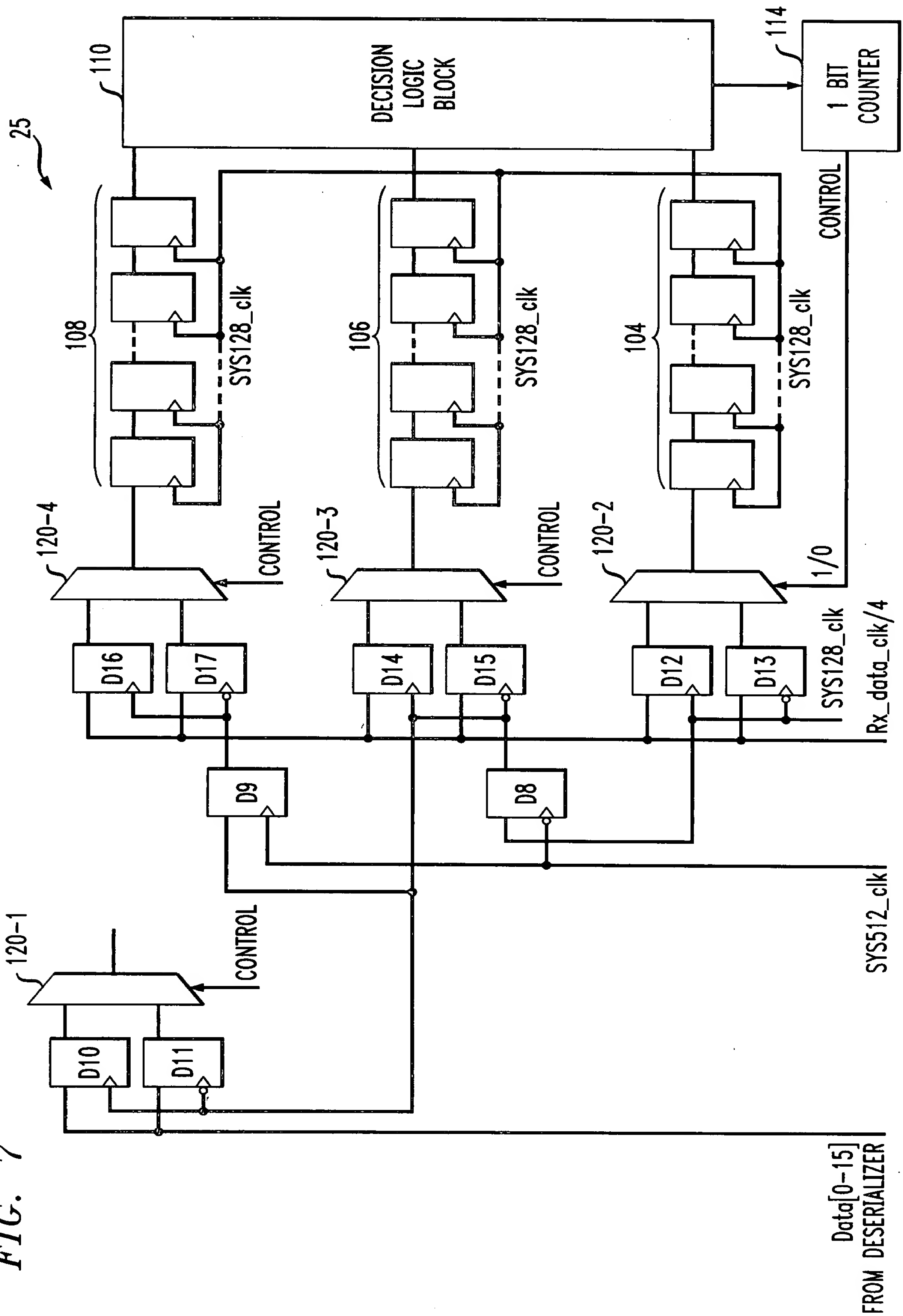


FIG. 6

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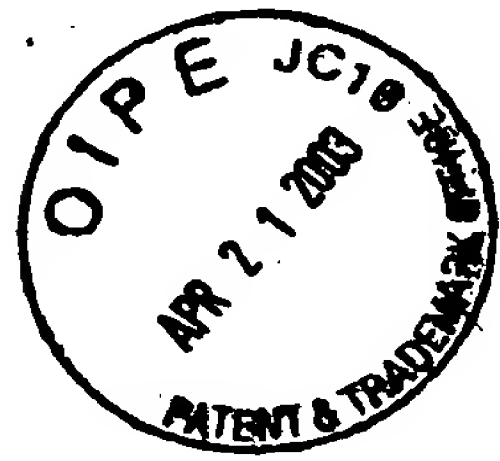
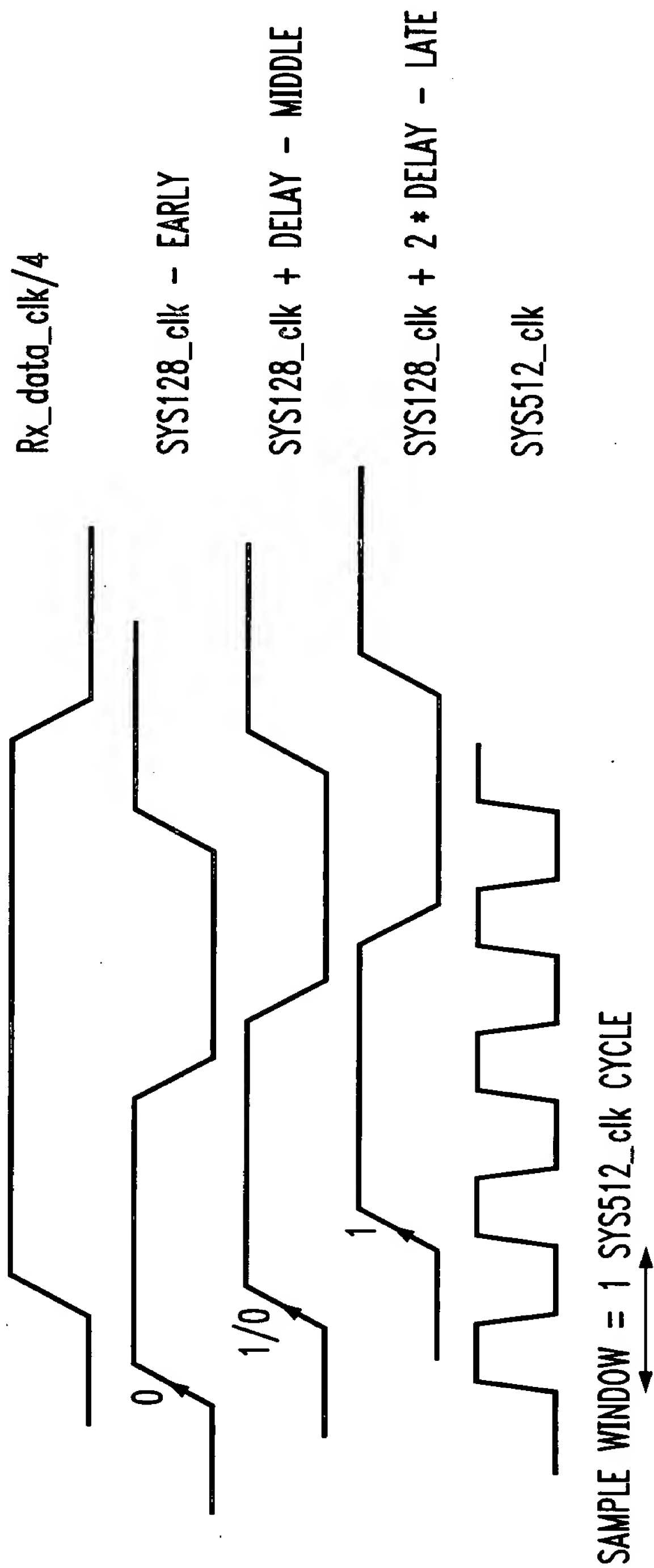
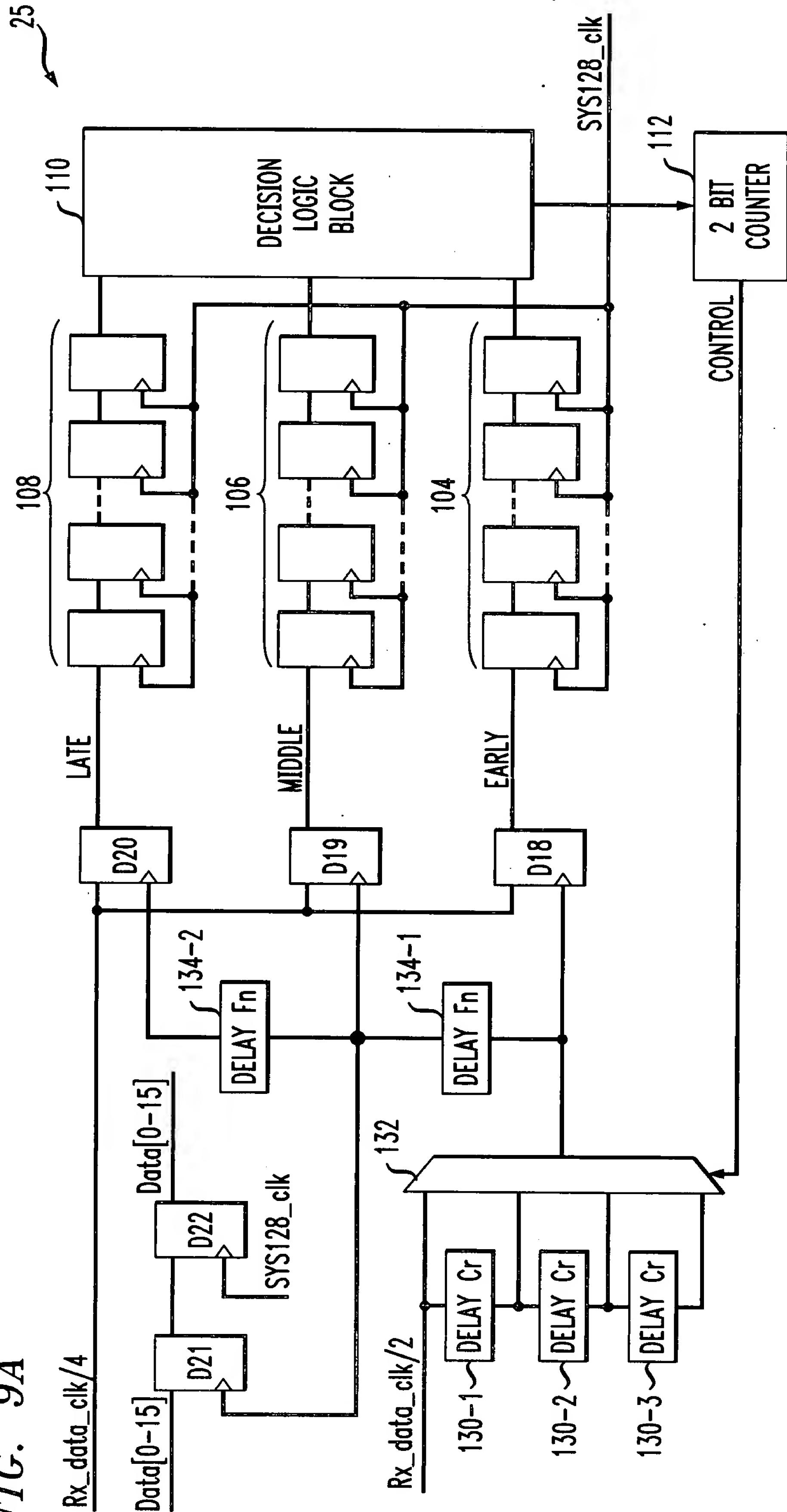


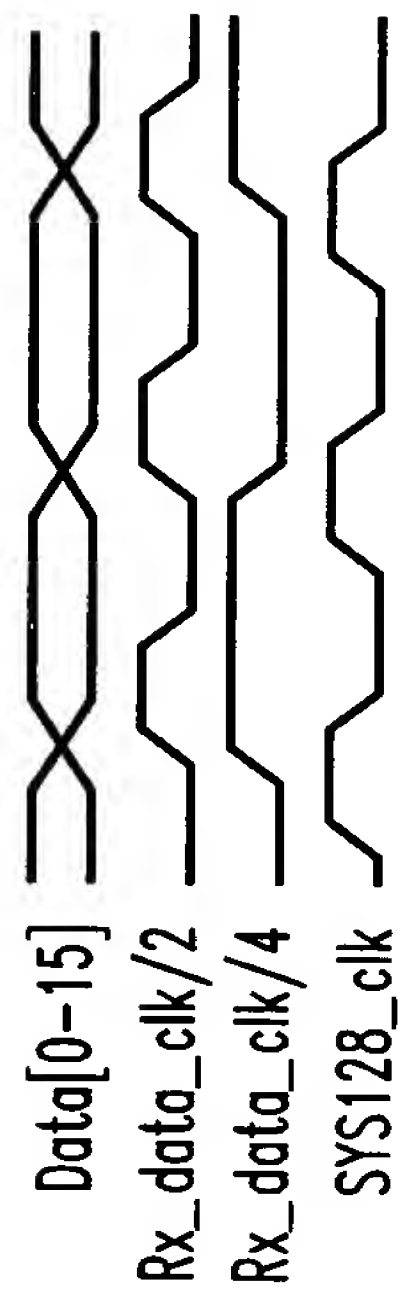
FIG. 8



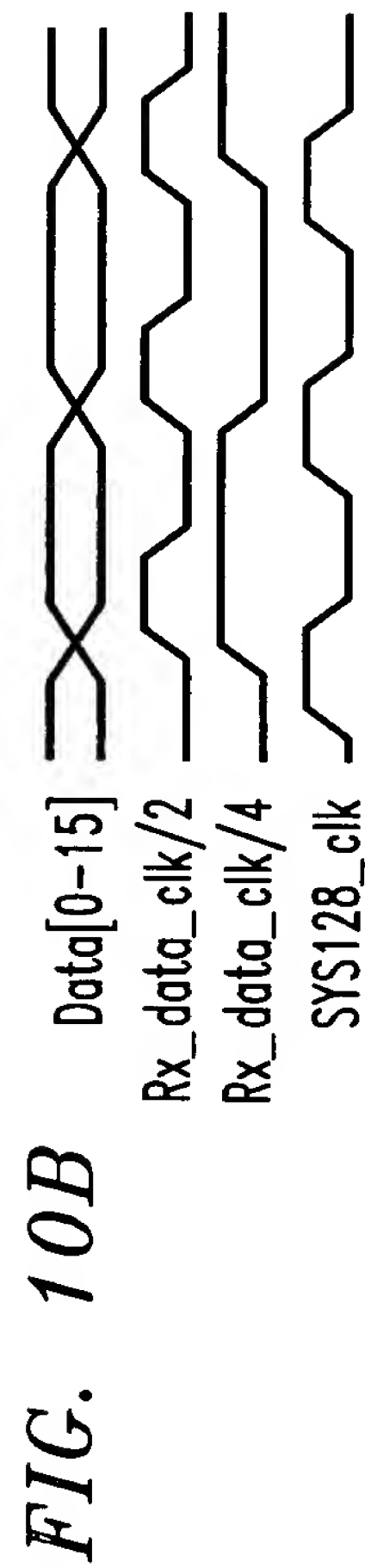
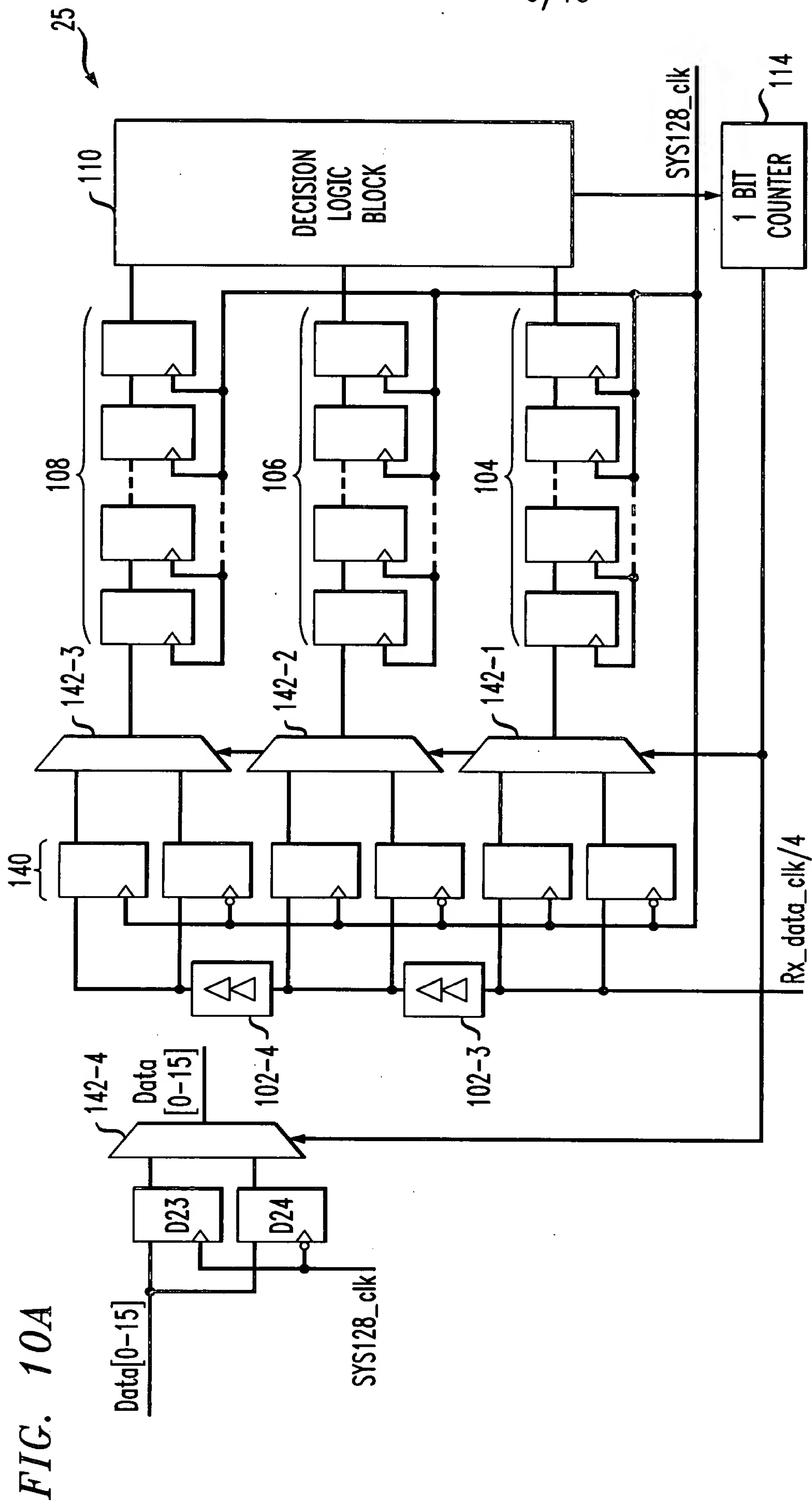
**FIG. 9A**



**FIG. 9B**









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FIG. 11B

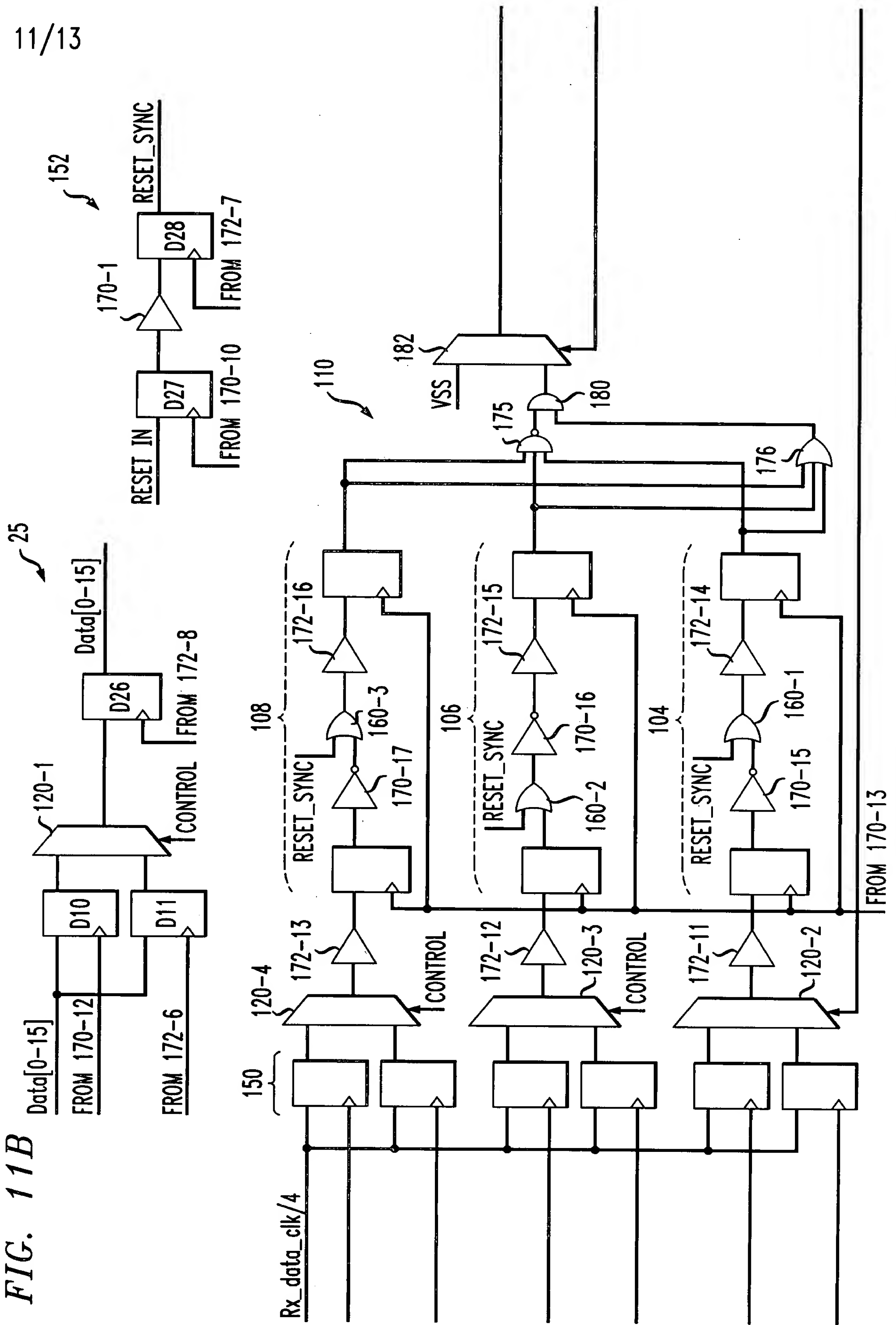


FIG. 11A	FIG. 11B	FIG. 11C
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Logic diagram of a reset circuit 114. The circuit includes a RESET\_SYNC input, a feedback loop from output 170-13, and a feedback loop from output 154. The circuit contains several logic gates (AND, OR, NOT) and flip-flops (D31, D30, D29, D32). The output of the circuit is 170-3.



FIG. 12

